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A TIGHTLY COUPLED AND SCALABLE MEMORY AND EXECUTION UNIT ARCHITECTURE

ABSTRACT OF THE DISCLOSURE

An architecture is shown where an execution unit is tightly coupled to a shared, reconfigurable memory system. Sequence control signals drive a DMA controller and address generator to control the transfer of data from the shared memory to a bus interface unit (BIU). The sequence control signals also drive a data controller and address generator which controls transfer of data from the shared memory to an execution unit interface (EUI). The EUI is connected to the execution unit operates under control of the data controller and address generator to transfer vector data to and from the shared memory. The shared memory is configured to swap memory space in between the BIU and the execution unit so as to support continuous execution and I/O. A local fast memory is coupled to the execution unit. A local address generator controls the transfer of scalar data between the local fast memory and the execution unit. The execution unit, local fast memory and local address generator form a fast memory path that is not dependent upon the slower data path between the execution unit and shared memory. The fast memory path provides for fast execution of scalar operations in the execution unit and rapid state storage and retrieval for operations in the execution unit.